

MEMORY CELL FOR MODIFICATION OF REVISION IDENTIFIER IN AN INTEGRATED CIRCUIT CHIP

ABSTRACT OF THE DISCLOSURE

A memory cell for reducing the cost and complexity of modifying a revision identifier (ID) or default register values associated with an integrated circuit (IC) chip, and a method for manufacturing the same. The cell, which may be termed a "Meta-Memory Cell" (MMCEL), is implemented on metal layers only and utilizes a dual parallel metal ladder structure that traverses and covers each metal and via layer from the bottom to the top of the metal layer structure of the chip. One of the metal ladders is connected to a power supply at the bottom metal layer, corresponding to a logic 1, and another metal ladder is connected to ground at the bottom metal layer, corresponding to a logic 0. The output of the MMCEL can thus be inverted at any metal or via layer and can be inverted as often as required. Significant cost savings are achieved because a revision ID or default register bits may be modified by altering only those metal layers where design changes are necessary.

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